ECR #: 40
Title: Change AGP-2X Mode t_{Dva} Spec
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Summary: The data valid after strobe specification (t_{Dva}) from the transmitter is being changed from 1.7 ns to 1.9 ns.

Background: Recent simulation of the bus have shown that there is less hold time margin on the A.G.P. bus than setup time margin. This is due to the extra 2.0 pF of capacitance allowed on the Strobe pins relative to the data pins. (Δ Cin - Strobe to data Pin Capacitance delta is -1.0 to +2.0 pF). About 200 ps of extra hold time is needed to balance the setup and hold times and give the maximum trace lengths.

There are several means to get 200 ps extra hold time. The 200 ps margin can be designed into both setup and hold times. The data clock can be delayed very slightly relative to the strobe clock to get an appropriate asymmetrical timing. However, all designs should already have the necessary additional margin for hold time by virtue of the skew allocation for simultaneous switching outputs (SSO) pushout delay. SSO pushout only increases the delay of a buffer, never decreases it. Thus, it decreases the data valid before strobe (t_{Dvb}) time without decreasing the t_{Dva} time. Therefore, if a design has allocated at least 200 ps for SSO pushout, then the additional margin for t_{Dva} is already present in that design. Most designs should be allocating between 400 and 600 ps for SSO pushout.

This change is accompanied with a discussion of SSO pushout for the design guide to make clear that this does not change most designs.

Change Current Specification as shown:

In table 4.4, edit the t_{Dva} spec as shown and add Note 1.

Symbol	Parameter	Min	Max	Units	Notes
Transmitter Output Signals:					
t_{Dva}	Data valid after strobe	1.9		ns	1

NOTES:
1. The asymmetry between data valid before and after strobe does not necessarily require any special design effort. See the A.G.P. Design Guide for more details.

Add Section to A.G.P. Design Guide as shown:

A new section on timing allocation is being added to the Design Guide to cover SSO pushout, as show below:

System Timing Considerations

The timings for AGP-1X mode are based on a common clock and are driven by input and output delays and the clock skew between the AGP components. The timings for AGP-2X are based on the skew between the strobe and data lines. A summary of the key elements are given in Table 1.

Table -1 A.G.P. Timing Elements

	AGP-1X (Delay)	AGP-2X (Skew)	Units
Clock Skew	1.0	(n.a.)	ns
Transmitter	6.0[1]	2.05	ns
Interconnect	2.5	0.70	ns
Receiver	5.5[1]	1.00[2]	ns
Total	**15**	**3.75**	**ns**

Note 1: Data timings
Note 2: Receiver Setup time

The delays of AGP-1X add up to one A.G.P. clock period (15 ns), the maximum time allowed for a data transfer. The skews of AGP-2X add up to a quarter of an A.G.P. clock period (3.75 ns), the nominal phase difference between a data transition and a strobe transition. The AGP-2X timings are affected by anything which causes a difference in the delays between data and strobe for the transmitter and interconnect, and in the receiver setup time. Some of these components and example values[1] are shown in Table 2 and Table 3.

Most of the components of the AGP-1X timings should be familiar to designers with experience in I/O design, especially PCI I/O design. The AGP-1X timings will not be discusses in detail here. However, it is important to be sure that all causes of delay and skew are included, such as clock jitter and simultaneous switching outputs (SSO) pushout delay.

All the components of the AGP-2X timings need to be carefully considered since there is much less timing margin in this case and several small contributions add up fast. The magnitudes of the AGP-2X component timings are smaller since they are generally the mismatched delays (skew) of two paths. Since the paths are made of the same or very similar circuits, the skew can be minimized if care is taken. AGP-2X designs use new bus techniques, so the timing components are likely to be less well understood. These components will be covered in more detail below. The timings for the interconnect are covered in full detail in the last sections of this chapter and in Chapter 2 and will not be covered further in this section.

The transmitter is assumed to use a PLL to produce a 50% duty cycle, 133 MHz clock needed to produce the required relative timings of data and strobe. Other timing generators can also be used for this purpose and identical timing considerations can be applied to them. The PLL is the primary source for the data / strobe clock jitter and clock duty cycle skew components. A 50% duty cycle clock provides the best balance of data to strobe setup and hold times. Any error in the clock duty cycle or any clock jitter reduces the time from the data to strobe (setup time) or strobe to data (hold time).

[1] The timings values shown in Table 2, Table 3, and other similar examples in this section are given to illustrate how the timing elements might be built, and are not meant as design recommendations.

Table 2 Example AGP-1X timing element components

Element	Delay Component [1]	AGP-1X	Units
Transmitter	Internal clock delay	1.0 [2]	ns
	Clock jitter	0.25	
	Clock to output delay	4.25	
	SSO pushout	0.5	
	Total	**6.0**	**ns**
Interconnect [3]	Longest line flight time	2.05	ns
	Crosstalk	0.45	
	Total	**2.50**	**ns**
Receiver	Input buffer delay	1.5	ns
	Input logic and routing delay	4.5	
	Data register setup time	0.5	
	Internal clock delay	-1.0 [2]	
	Total	**5.5**	**ns**

Table 3 Example AGP-2X timing element components

Element	Skew Component [1]	AGP-2X	Units
Transmitter	Data / strobe clock jitter	0.25	ns
	Data / strobe clock duty cycle	0.20	
	Internal data clock skew	0.10	
	Buffer delay matching	0.25	
	Rise / Fall time matching	0.75	
	SSO pushout	0.50	
	Total	**2.05**	**ns**
Interconnect [3]	Data / Strobe trace mismatch	0.10	ns
	Capacitive loading mismatch	0.15	
	Crosstalk	0.45	
	Total	**0.70**	**ns**
Receiver	Strobe to data path skew	0.9	ns
	Strobe routing skew	0.1	
	Total	**1.0**	**ns**

Note 1: These components do not include testing guardband allowances that may be required for production testing.
Note 2: The internal clock delay acts to delay outputs, but assists on input setup times.
Note 3: Interconnect delays and skews are for motherboard and add-in card combined.

The PLL has an intrinsic jitter caused by jitter in its clock source, by supply noise, crosstalk with digital signals on the same chip and sometimes from sources within the PLL itself. Jitter can be reduced by providing a low jitter clock source and by proper isolation and bypassing of the power to the PLL. The PLL may output a good clock duty cycle with the voltage controlled oscillator (VCO) running at 133 MHz. If the duty cycle is not close to 50%, it may be necessary to run the VCO at 266 MHz and divide by 2. Clock duty cycle is also affected by internal loading and buffering of the clock. The 133 MHz clock path should be carefully constructed and simulated to insure the fidelity of the signal throughout the AGP-2X interface.

The 133 MHz clock also has to be routed to all outputs of the interface and proper care needs to be taken such that the clock skew across the interface is minimized. Automatic clock tree synthesis may provide insufficient skew control. Manual placement and routing gives better results. Also, the timing registers for the outputs can be built into a custom I/O buffer.

The buffer itself needs to be carefully designed to balance the delays to the rising and falling edges. This is typically one of the bigger components of transmitter skew. Any delay mismatch reduces data setup and hold time margin.

The other big transmitter skew component is SSO pushout. When a group of outputs switched in the same direction at the same time, the output delay of the buffer slows a bit due to internal ground or power line voltage drop (resistive and inductive effects). While, all other skews are equally likely to reduce setup or hold time, SSO is different in that it only causes data delay and it cannot cause the signal to occur earlier. This means that SSO only affects data setup time. (It affects AGP-1X the same way by increasing the clock to output delay of the buffer.)

SSO pushout can be reduced by increasing the number of ground and power connections to the output buffers (reducing the supply resistance and inductance). However, at some point this adds to device packaging cost. SSO pushout also be reduced by designing the buffers to the weak end of the buffer strength spec with the largest allowed rise and fall times, consistent with meeting the AGP-1X output delay specs. This reduces the buffer di/dt and, consequently, the inductive component of power supply voltage drop.

All buffer designs will suffer some level SSO pushout. One consequence of SSO pushout is that data hold time is always longer than data setup time. Because of this asymmetry, the AGP-2X data hold time after strobe (tDva) is specified to be 200 ps more than the data setup time before strobe (tDvb) (see table 4-4 in the A.G.P. Specification). This establishes 200 ps as the minimum allowance for SSO pushout. (Any pushout allowance greater than 200 ps does not change the specifications for data valid time after strobe).

The receiver setup and hold timings are most affected by the matching of the data input path delay to the strobe input path delay. Because the strobe serves many data inputs, its input buffer is more heavily loaded. This usually results in more delay and must be compensated for in the data path. Each strobe control spans half the data inputs, and the skew of the strobe arriving at each data input should be well matched. The strobe buffer should be located physically in the center of the data pins it serves. Strobe input buffer loading can be reduced by providing one or more input buffers distributed through the interface, all driven from the same strobe input pad. While this can reduce loading effects and skews, care has to be taken that the capacitive load of the strobe (including packaging) is within the range of -1.0 pF to +2.0 pF as compared to the capacitive load of all data pins connected with that strobe.

Reducing the range of input sense levels also reduces the setup and hold time skew. As mentioned above, using differential input buffers can reduce the sense level uncertainty. Also, the input buffer power supplies should be clean of noise and well bypassed and the external VREF, if used, must be well bypassed to suppress noise.